CLAIMS

We claim:

1. A method for fast localization of electrically measured defects of integrated circuits, comprising:

(a) providing information for fabricating a test chip having test structures configured for parallel electrical testing;

(b) electrically testing the test structures on the test chip employing a parallel electrical tester; and

(c) analyzing results of the electrical testing to localize defects on the test chip.

2. The method of claim 1, further comprising:

inspecting the localized defects on the test chip using an inspection tool.

3. The method of claim 2, wherein the inspection tool is a scanning electron microscope (SEM).

4. The method of claim 3, further comprising:

sizing the test structures on the test chip to be compatible with a view field of the SEM.

5. The method of claim 1, further comprising:

grouping the test structures into one or more padgroups, wherein the test structures in a padgroup are electrically tested together in parallel.

6. The method of claim 5, wherein a padgroup includes:

two columns of test structures; and

two columns of pads disposed between the two columns of test structures.

7. The method of claim 5, further comprising:

grouping padgroups into one or more sticks, wherein the padgroups in a stick are electrically tested together in parallel.

8. The method of claim 7, wherein the padgroups in a stick are electrically tested together in parallel using a probe card connected to the parallel electrical tester.

9. The method of claim 8, wherein one or more cells having test structures and corresponding pads are disposed between two padgroups in a stick, wherein the one or more cells are used to verify the operation of the probe card.

10. The method of claim 7, further comprising:
stacking two or more sticks together in a layout.

11. The method of claim 10, further comprising:
adjusting the number of sticks stacked together in the layout to fit within a scanner field.

12. The method of claim 1, further comprising:
in-line inspecting the test chip using an optical inspection tool.

13. The method of claim 1, wherein the test chip includes a plurality of design pattern variations.

14. The method of claim 1, wherein the test structures are two-terminal or four-terminal test structures.

15. The method of claim 1, wherein one of the test structures is a snakecomb cell configured to localize a defect in the snakecomb cell to a location within the snakecomb cell.

16. The method of claim 1, wherein electrically testing includes:
comparing a line resistance to a first threshold resistance, wherein the line resistance is determined based on a measured voltage;
when the line resistance is below the first threshold voltage, detecting a soft short;
comparing the line resistance to a second threshold resistance; and
when the line resistance is below the second threshold resistance, detecting a hard short, wherein the first threshold resistance is greater than the second threshold resistance.

17. The method of claim 1, wherein electrically testing includes:

determining an average resistance for a number of lines adjacent to each other;

comparing a line resistance to the average resistance;

when the line resistance is less than the average resistance by a first specified amount, detecting a soft short; and

when the line resistance is less than the average resistance by a second specified amount, detecting a hard short, wherein first specified amount is less than the second specified amount.

18. The method of claim 1, wherein the parallel electrical tester is connected to a wafer loader and a wafer prober, and further comprising:

loading one or more test chips from the wafer loader into the wafer prober to be tested, and wherein the wafer prober includes a probe card to electrically contact the test structures on the test chip to be electrically tested in parallel.

19. The method of claim 18, further comprising:

transmitting test signals between the probe card and a pin termination module in the parallel electrical tester;

transmitting test signals between the pin termination module and a measurement control module in the parallel electrical tester; and

transmitting commands to the wafer prober from a tester control module in the parallel electrical tester.

20. The method of claim 19, further comprising:

transmitting voltage sources and control signals from the measurement control module to the pin termination module.

21. The method of claim 19, further comprising:

receiving test signals from the probe card at a plurality of switch cards in the pin termination module, wherein each switch card is connected to a group of pins from the probe card.

22. The method of claim 21, wherein a switch card forms a resistor divider with a resister in a test structure, a termination resistor, and a voltage source.

23. The method of claim 21, wherein a switch card includes:

a plurality of pin terminator circuits, wherein each pin terminator circuit is connected to a pin from the probe card; and

a plurality of digital multiplexer controls, wherein each digital multiplexer control is connected to two pin terminator circuits.

24. The method of claim 23, wherein a pin terminator circuit includes a plurality of quad switches, wherein each quad switch is connected to a voltage source and control signals.

25. The method of claim 19, further comprising:

receiving test signals from the probe card at a multiplexer module in the measurement control module;

combining a set of test signals received from the probe card into a digital acquisition signal; and

transmitting the digital acquisition signal to a digital acquisition card.

26. The method of claim 1, wherein analyzing results comprises:

classifying detected defects as random or systematic defects.

27. The method of claim 26, further comprising:

grouping test chip design patterns into layout bins; and

plotting failure counts for each layout bin.

28. A system for fast localization of electrically measured defects of integrated circuits, comprising:

(a) a test chip having test structures configured to be parallel electrically tested;

(b) a parallel electrical tester configured to parallel electrically test the test structures on the test chip; and

(c) a processor configured to analyze results from the parallel electrical tester to localize defects on the test chip.

29. The system of claim 28, further comprising:

an inspection tool configured to inspect the localized defects on the test chip.

30. The system of claim 29, wherein the inspection tool is a scanning electron microscope (SEM).

31. The system of claim 30, wherein the test structures on the test chip are sized to be compatible with a view field of the SEM.

32. The system of claim 28, wherein the test structures are grouped into one or more padgroups, wherein the test structures in a padgroup are electrically tested together in parallel.

33. The system of claim 32, wherein a padgroup includes:
two columns of test structures; and
two columns of pads disposed between the two columns of test structures.

34. The system of claim 32, wherein padgroups are grouped into one or more sticks, wherein the padgroups in a stick are electrically tested together in parallel.

35. The system of claim 34, wherein the padgroups in a stick are electrically tested together in parallel using a probe card connected to the parallel electrical tester.

36. The system of claim 35, wherein one or more cells having test structures and corresponding pads are disposed between two padgroups in a stick, wherein the one or more cells are used to verify the operation of the probe card.

37. The system of claim 34, wherein two or more sticks are stacked together in a layout.

38. The system of claim 37, wherein the number of sticks stacked together in the layout is adjusted to fit within a scanner field.

39. The system of claim 28, further comprising:
an optical inspection tool to in-line inspect the test chip.

40. The system of claim 28, wherein the test chip includes a plurality of design pattern variations.

41. The system of claim 28, wherein the test structures are two-terminal or four-terminal test structures.

42. The system of claim 28, wherein one of the test structures is a snakecomb cell configured to localize a defect in the snakecomb cell to a location within the snakecomb cell.

43. The system of claim 28, wherein test structures are placed at more than one level.

44. The system of claim 43, wherein test structure below a test structure on another level is electrically tested.

45. The system of claim 43, wherein the interaction of test structures at two different levels is measured.

46. The system of claim 28, wherein the parallel electrical tester is configured to:

compare a line resistance to a first threshold resistance, wherein the line resistance is determined based on a measured voltage;

when the line resistance is below the first threshold voltage, detect a soft short;

compare the line resistance to a second threshold resistance; and

when the line resistance is below the second threshold resistance, detect a hard short, wherein the first threshold resistance is greater than the second threshold resistance.

47. The system of claim 28, wherein the parallel electrical tester is configured to:

determine an average resistance for a number of lines adjacent to each other;

compare a line resistance to the average resistance;

when the line resistance is less than the average resistance by a first specified amount, detect a soft short; and

when the line resistance is less than the average resistance by a second specified amount, detect a hard short, wherein first specified amount is less than the second specified amount.

48. The system of claim 28, wherein the parallel electrical tester is connected to a wafer loader and a wafer prober, wherein the wafer loader loads one or more test chips into the wafer prober to be tested, and wherein the wafer prober includes a probe card to electrically contact the test structures on the test chip to be electrically tested in parallel.

49. The system of claim 48, wherein the parallel electrical tester includes:

a pin termination module connected to the probe card, wherein test signals are transmitted between the pin termination module and the probe card;

a measurement control module connected to the pin termination module, wherein test signals are transmitted between the pin termination module and the measurement control module; and

a tester control module connected to the measurement control module and the wafer prober, wherein the tester control module sends commands to the wafer prober.

50. The system of claim 49, wherein the measurement control module provides voltages source and control signals to the pin termination module.

51. The system of claim 48, wherein the pin termination module includes:

a plurality of switch cards to receive test signals from the probe card, wherein each switch card is connected to a group of pins from the probe card.

52. The system of claim 48, wherein a switch card forms a resistor divider with a resister in a test structure, a termination resistor, and a voltage source.

53. The system of claim 51, wherein a switch card includes:

a plurality of pin terminator circuits, wherein each pin terminator circuit is connected to a pin from the probe card; and

a plurality of digital multiplexer controls, wherein each digital multiplexer control is connected to two pin terminator circuits.

54. The system of claim 53, wherein a pin terminator circuit includes a plurality of quad switches, wherein each quad switch is connected to a voltage source and control signals.

55. The system of claim 49, wherein the measurement control module includes:

a multiplexer module that receives test signals from the probe card; and

a digital acquisition card, wherein the multiplexer module combines a set of test signals received from the probe card into a digital acquisition signal sent to the digital acquisition card.

56. The system of claim 28, wherein the processor is configured to:

classify detected defects as random or systematic defects.

57. The system of claim 56, wherein the processor is configured to:

group test chip design patterns into layout bins; and

plot failure counts for each layout bin.

58. A computer-readable storage medium containing computer executable code to instruct a computer to localize electrically measured defects of integrated circuits by instructing the computer to operate as follows:

(d) providing information for fabricating a test chip having test structures configured for parallel electrical testing;

(e) electrically testing the test structures on the test chip employing a parallel electrical tester; and

(f) analyzing results of the electrical testing to localize defects on the test chip.